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(54) Substrate polishing method and apparatus

(57) A method and apparatus provides a method for polishing a surface of a substrate with a polishing pad (212). The surface of the substrate (204) is polished using the polishing pad (212) and the surface of the substrate (204) is deformed in response to changes in the polishing pad (212), wherein deformation of the surface of the substrate (204) increases uniformity in polishing of the surface of the substrate (204).

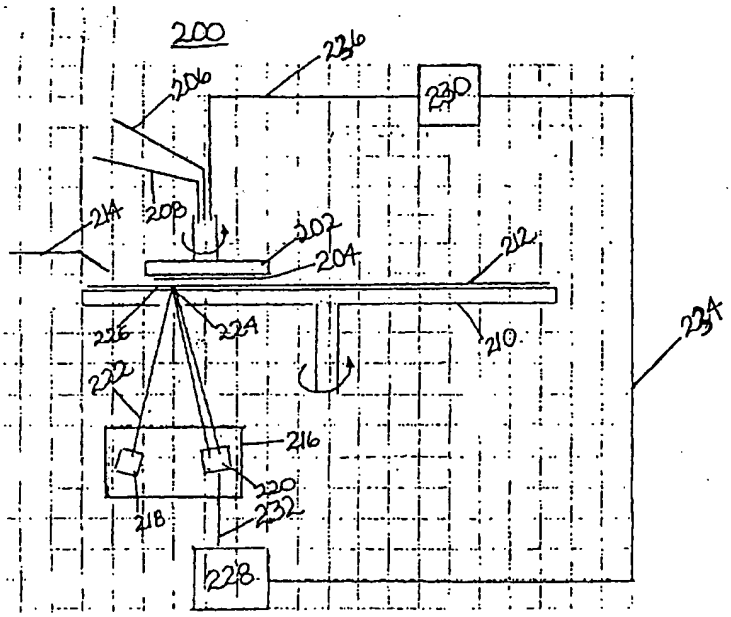


FIG. 2

Description

[0001] The present invention relates generally to the manufacturing of semiconductor devices, and in particular to chemical mechanical polishing of substrates.

[0002] In certain technologies, such as integrated circuit fabrication, optical device manufacture and the like, it is often crucial to the fabrication processes involved that the workpiece from which the integrated circuit, optical, or other device is to be formed have a substantially planar front surface and, for certain applications, have both a planar front surface and back surface.

[0003] One process for providing such a planar surface is to scour the surface of the substrate with a conformable polishing pad, commonly referred to as "mechanical polishing". When a chemical slurry is used in conjunction with the pad, the combination of slurry and pad generally provides a higher material removal rate than is possible with mere mechanical polishing. This combined chemical and mechanical polishing, commonly referred to as "CMP", is considered an improvement over mere mechanical polishing processes for planarizing or polishing substrates. The CMP technique is common for the manufacture of semiconductor wafers used for the fabrication of integrated circuit die.

[0004] Chemical-mechanical polishing (CMP) is performed in the processing of semiconductor wafers and/or chips on commercially available polishers, such as the Westech 372/372M polishers. The standard CMP tools have a circular polishing table and a rotating carrier for holding the substrate.

[0005] Difficulties exist ensuring uniformity of polishing of a substrate, such as a silicon wafer using CMP processes. For example, in Figure 1, a portion of CMP tool 100 is illustrated. CMP tool 100 includes a wafer carrier 102, which provides a vacuum and back pressure through plenum area 104 and holes 106. A vacuum is employed to cause surface 108 of substrate 110 to adhere to wafer carrier 102. CMP tool 100 also includes a primary polish pad 112, which is coupled to primary platen 114. Both wafer carrier 102 and primary platen 114 rotate during CMP processes to polish surface 116 of substrate 110. During rotation, rebound, and other dynamics involving primary polish pad 112 results in deformities of primary polish pad 112, as shown in section 118 of primary polish pad 112. These deformities, resulting from factors, such as pad rebound, result in lower polish rates near edge 120 of substrate 110. Higher polish rates occur just inside edge 120 of substrate 110. In particular, valley 122 and valley 124 result in less polishing occurring in section 126 and section 128 of polish surface 116. Therefore, it would be advantageous to have an improved method and apparatus for CMP that provides for more uniformity of the substrate surface from polishing of the substrate.

[0006] The present invention seeks to provide a method and apparatus for polishing the surface, for example a substrate, that exhibits advantages over known methods and apparatus.

[0007] In accordance with one aspect of the present invention there is provided a method of polishing a surface of a substrate with a polishing pad, characterized by the steps of detecting deformations in the polishing pad, and deforming the surface of the substrate in response to deformations in the polishing pad wherein deformation of the surface of the substrate increases uniformity in polishing of the surface of the substrate.

[0008] In accordance with another aspect of the present invention there is provided a substrate polishing apparatus comprising polishing means for polishing the surface of a substrate by means of a polishing pad, detection means for detecting deformation of the polishing pad, deformation means for deforming the surface of the substrate responsive to the deformation of the polishing pad, wherein deformation of the surface of the substrate increases uniformity in polishing of the surface of the substrate.

[0009] The invention is advantageous in allowing for the active adjustment of a substrate as part of a polishing procedure. The deformation means can thus comprise active deformation means such as, for example, at least one piezoelectric element.

[0010] The invention is described further hereinafter by way of example only, with reference to and as illustrated in the accompanying drawings in which:

Figure 2 is a CMP tool in accordance with a preferred embodiment of the present invention;
Figure 3 is a diagram of a portion of the CMP tool of Figure 2;
Figures 4A-4D are illustrations of configurations for displacement elements in accordance with a preferred embodiment of the present invention;
Figure 5 is a flowchart of a process for CMP using an electrically active wafer carrier system in accordance with a preferred embodiment of the present invention; and
Figure 6 is a flowchart of a process for adjusting the shape of the wafer during the polishing process in accordance with another embodiment of the present invention.

[0011] Process variables in the chemical mechanical polishing processing typically include: down-force, wafer carrier back-pressure, wafer carrier rotational speed, primary platen rotational speed, and polishing slurry flow. Selection of a given primary polishing pad leads to adjustment of process variables to achieve desired polishing responses. Uncontrolled variables are compensated for with the above listed parameters but still remain uncontrolled.

[0012] Using a standard wafer carrier, air pressure can be applied "behind" the wafer to effectively bow the wafer outward from the wafer carrier surface. This action is performed in an attempt to compensate for polishing non-uniformity. The fundamental problem with this

method is that air is a compressible fluid and the resulting "bubble" of air behind the wafer cannot be contained. It will be subject to drifting and its shape will be at best symmetrical to the center of the wafer carrier. No backpressure setting could be applied to completely compensate for the polish pad rebound effect.

[0013] The electrically active wafer carrier provided by the present invention allows control of the wafer shape to compensate for the uncontrolled variables that result from the flexibility of the primary polish pad. Additionally, the electrically active wafer carrier can compensate for wafer bow due to internal stress on the substrate being polished. These internal stresses occur from the stress mismatch between the variety of films deposited on the substrate to be polished prior to the polishing operation.

[0014] With reference now to the figures, and in particular with reference to Figure 2, a CMP tool is depicted in accordance with a preferred embodiment of the present invention. CMP tool 200 is an electrically active wafer carrier that is employed to provide adjustment to the shape of the wafer during CMP operations for improved wafer polishing uniformity. CMP tool 200 includes a wafer carrier 202, which is employed to hold substrate 204 for CMP operations. Wafer carrier 202 is designed to be rotated, which results in rotation of substrate 204. In the depicted example, substrate 204 adheres to wafer carrier 202 by the use of a vacuum applied to the back surface of substrate 204. Wafer carrier 202 includes a wafer carrier vacuum line 206, which provides a vacuum for causing substrate 204 to adhere to wafer carrier 202 during CMP operations. CMP tool 200 may be used to process a number of different types of substrates. Most commonly, CMP tool 200 is used to process a semiconductor wafer, such as a silicon wafer. Additionally, a wafer carrier back pressure air supply line 208 is connected to wafer carrier 202. Back pressure air supply line 208 supplies a specified pressure of air to counteract the bow induced by the wafer carrier vacuum used to hold the substrate in place on the wafer carrier. Both carrier vacuum and back pressure may be applied at the same time.

[0015] CMP tool 200 also includes a primary polish platen 210, which also rotates during CMP operations. Primary polish platen 210 holds primary polish pad 212 and rotates this polish pad during CMP operations. Polish slurry line 214 is employed to provide polish slurry, which is applied to primary polish pad 212 for CMP operations used to polish a substrate, such as substrate 204. Additionally, CMP tool 200 includes an in situ film thickness measurement unit 216, containing laser 218 and sensor 220, employed to measure film thicknesses during CMP operations. Alternatively, the CMP operation may be periodically halted for measuring film thicknesses using in situ film thickness measurement unit 216. In situ film thickness measurement unit 216 is a laser based interferometer or similar device based on an optical film thickness measurement. Coherent light beam 222 is passed through a window 224 in the primary polish platen 210 and a corresponding window 226 in primary polish pad 212. Coherent light beam 222 is reflected off substrate 204, through windows 224 and 226 and back to sensor 220 located under primary polish pad 212. In the depicted example, window 226 in primary polish pad 212 should be filled in with a flexible plastic or other similar material to provide a continuous surface for the polishing slurry to flow over during the polishing operation.

[0016] Measurements of film thicknesses are sent to film thickness/endpoint analysis and driver interface 228. The film thickness measurement system provides instantaneous film thickness measurements. These measurements when integrated over the surface of the wafer by time can be used to determine a rate of film removal. Additionally, the various removal rates can be used to determine uniformity by and removal rates by user defined zones. The zone data coupled with wafer carrier position data can be fed to an analysis unit within driver module 230. Driver module 230 then sends the appropriate signals to the piezoelectric element array/matrix resulting in the ideal wafer shape to achieve best polishing uniformity (sometimes referred to as polishing non-uniformity). (Lower non-uniformity values are more desirable). Measurements of film thicknesses are sent to film thickness/endpoint analysis and driver interface 228, which is connected to in situ film thickness measurement unit 216 by data line 232.

[0017] In turn, measurements of film thicknesses are sent to film thickness/endpoint analysis and driver interface 228 is connected to driver module 230 by data line 234. Driver module 230 provides control signals to a displacement unit containing a number of displacement units (not shown). In the depicted example, the displacement units are piezoelectric elements. The displacement unit is located within wafer carrier 202. These control signals are sent to the piezoelectric elements using control line 236, which couples driver module 230 to the piezoelectric elements located within wafer carrier 202. These control signals are employed to adjust the shape of a substrate, such as substrate 204 as it is processed through CMP.

[0018] In the depicted example, displacement units in the form of piezoelectric elements are used to make compensations, such as counteracting the inherent bow of a wafer, to insure the surface of the wafer is flat relative to the polishing pad. These piezoelectric elements also are employed to compensate for any bow in the wafer present to a variety of thermal processing and film stresses encountered by the wafer during semiconductor fabrication processes. This aids in compensating for the overall tendency to have slow center polish rates due to the inability of presently available systems to control the shape of the wafer with current vacuum holding mechanisms. Additionally, the piezoelectric elements also are used to adjust the surface of the wafer being polished to reduce effects from deformations in the pol-

ishing pad.

[0019] With reference now to Figure 3, a diagram of a portion of the CMP tool in Figure 2 is illustrated in accordance with a preferred embodiment of the present invention. Duplicate reference numerals are used in Figure 3 to identify corresponding elements from Figure 2. Wafer carrier 202 has substrate 204 attached to it in Figure 3. In the depicted example, substrate 204 is a semiconductor wafer. A vacuum is applied to substrate 204 through plenum connection 300, which provides the vacuum to hold substrate 204. As can be seen in this example, primary polish pad 212 has been altered in shape. In particular, deformations are present in section 302 of primary polish pad 212. This deformation of primary polish pad 212 may occur from a number of sources, such as, for example, pad rebound effect. This deformation in section 302 of primary polish pad 212 causes non-uniform polishing of polishing surface 304 in substrate 204.

[0020] Displacement unit 306 in the depicted example includes a number of piezoelectric elements 308, 310, 312, 314, and 316, which are used to temporarily deform or bend polishing surface 304 on substrate 204 in response to deformation of primary polish pad 212. Piezoelectric elements 308, 310, 312, 314, and 316, which are coupled to driver module 230 by electrical interface 318. Piezoelectric elements 308 and 316 are in a positive deflection mode, which are used to shape substrate 204. Piezoelectric element 312 is in a negative deflection mode and also is being employed to shape substrate 204. Piezoelectric elements 310 and 314 are in a neutral state in the depicted example.

[0021] The bending or deformation of polishing surface 304 is such that uniform polishing of polishing surface 304 and substrate 204 occurs even though the shape of primary polishing pad 212 has been altered. As can be seen in Figure 3, polishing surface 304 of substrate 204 has been deformed or bent to compensate for low regions 320 and 322 within section 302 of primary polishing pad 212 to minimize the effect of deformation of primary polishing pad 212.

[0022] With reference to Figures 4A-4D, illustrations of configurations for displacement elements are depicted in accordance with a preferred embodiment of the present invention. These figures depict how displacement elements, such as piezoelectric elements would be arranged within a wafer carrier. The figures show the arrangement on the surface of the carrier that would be used to hold and bend or deform a substrate, such as a semiconductor wafer. In Figure 4A, wafer carrier 400 contains concentric rings of piezoelectric elements. In particular, in the depicted example in Figure 4A, wafer carrier 400 contains concentric rings 402, 404, 406, 408, and 410. In Figure 4B, wafer carrier 412 contains interleaved fingers of piezoelectric elements. These piezoelectric elements are found in "fingers", such as in sections 414, 416, 418, and 420. A grid array 422 containing independent piezoelectric elements are employed within carrier 424 in Figure 4C. In Figure 4D, carrier 426 contains concentric rings similar to those used in carrier 402 in Figure 4A. The concentric rings in carrier 426, however, are segmented into sections 428. Although Figures 4A-4D illustrate specific examples of configurations for piezoelectric elements, any variety of geometric shapes or density of piezoelectric elements may be employed as necessary to achieve the desired shaping of the substrate.

[0023] Turning now to Figure 5, a flowchart of a process for CMP using an electrically active wafer carrier system is depicted in accordance with a preferred embodiment of the present invention. The process begins by placing all piezoelectric elements in a neutral position (step 500). Polishing of a pilot wafer then begins (step 502). The pilot wafer is the first wafer in a batch and is used to determine settings for the other wafers in the batch. A diameter measurement scan of the polished wafer is performed (step 504). The diameter scan data is analysed to identify regions of high and low removal rates (step 506). This step is performed using an off line analysis package. The data is used to obtain appropriate settings to drive the piezoelectric elements in the electrically active wafer carrier (step 508). The wafer is then polished using the settings to achieve desired uniformity in the wafer (step 510). If total film thickness and polishing uniformity are acceptable, then the current settings are used to polishing additional wafers in the batch. Otherwise, use new settings from the analysis to polish other wafers in the batch.

[0024] With reference now to Figure 6, a flowchart of a process for automatically adjusting the shape of the wafer during the polishing process is depicted in accordance with a preferred embodiment of the present invention. The process in Figure 6 requires an ability to measure the surface of the wafer being polished during the polishing process. This may be achieved using an electrically active wafer carrier such as the one depicted in Figure 2. The process begins by polishing the wafer (step 600). As the wafer is being polished, removal rate data is gathered using an apparatus, such as in situ film thickness measurement unit 216 in Figure 2 (step 602). Data is analysed for wafer location and uniformity (step 604). The position and uniformity data is converted into address data, which is used to adjust the appropriate piezoelectric elements to achieve the desired uniformity. This analysis would be made using driver interface 228 in Figure 2. The position and uniformity data is converted into driver data and sent to driver module 230, which adjusts the piezoelectric elements to change the shape of the wafer (step 606). Using this process, the shape of a substrate may be changed while it is being polished without requiring the polishing process to be interrupted for measurements as in Figure 5.

[0025] Therefore, the present invention provides an improved method and apparatus for providing adjustments to a substrate to compensate for factors, such as the bow introduced by the vacuum used to hold the sub-

strate in the carrier as well as for changes in the shape of the polishing pad used during the CMP. By changing the shape of the polishing surface of the substrate in response to changes in the shape of the polishing pad, the method and apparatus of the present invention provides for improved uniformity in the polishing surface of the substrate during the polishing operation. Thus, the present invention provides an advantage over presently available systems by solving problems such as those associated with bending of the wafer and changes to the shape of the polishing pad caused by pad rebound effect. The present invention also solves problems associated with stresses that result from processing of the wafer.

Claims

1. A method of polishing a surface of a substrate (204) with a polishing pad (212), characterized by the steps of:

   detecting deformations in the polishing pad (212) ; and
   deforming the surface of the substrate (204) in response to deformations in the polishing pad (212) wherein deformation of the surface of the substrate (204) increases uniformity in polishing of the surface of the substrate (204).

2. A method as claimed in Claim 1, wherein the step of deforming the surface of the substrate (204) is accomplished by means of a plurality of piezoelectric elements.

3. A method as claimed in Claim 1 or 2, wherein the detecting step comprises interrupting the polishing step and taking a measurement relative to the surface of the substrate (204).

4. A method as claimed in Claim 1 or 2, wherein the detecting step comprises taking a measurement relative to the surface of the substrate (204) during the polishing step.

5. Substrate polishing apparatus (200) comprising:

   polishing means (202, 210) for polishing the surface of a substrate (204) by means of a polishing pad (212);
   detection means (216) for detecting deformation of the polishing pad (212) ; and
   deformation means (308, 310, 312, 314, 316) for deforming the surface of the substrate (204) responsive to the deformation of the polishing pad (212), wherein deformation of the surface of the substrate increases uniformity in polishing of the surface of the substrate.

6. Apparatus as claimed in Claim 5, wherein the polishing means (202, 210) includes a carrier for the substrate (204) and the deformation means comprises a deformation unit (306) located within the carrier and arranged to selectively deform the surface of the substrate.

7. Apparatus as claimed in Claim 6, further comprising:

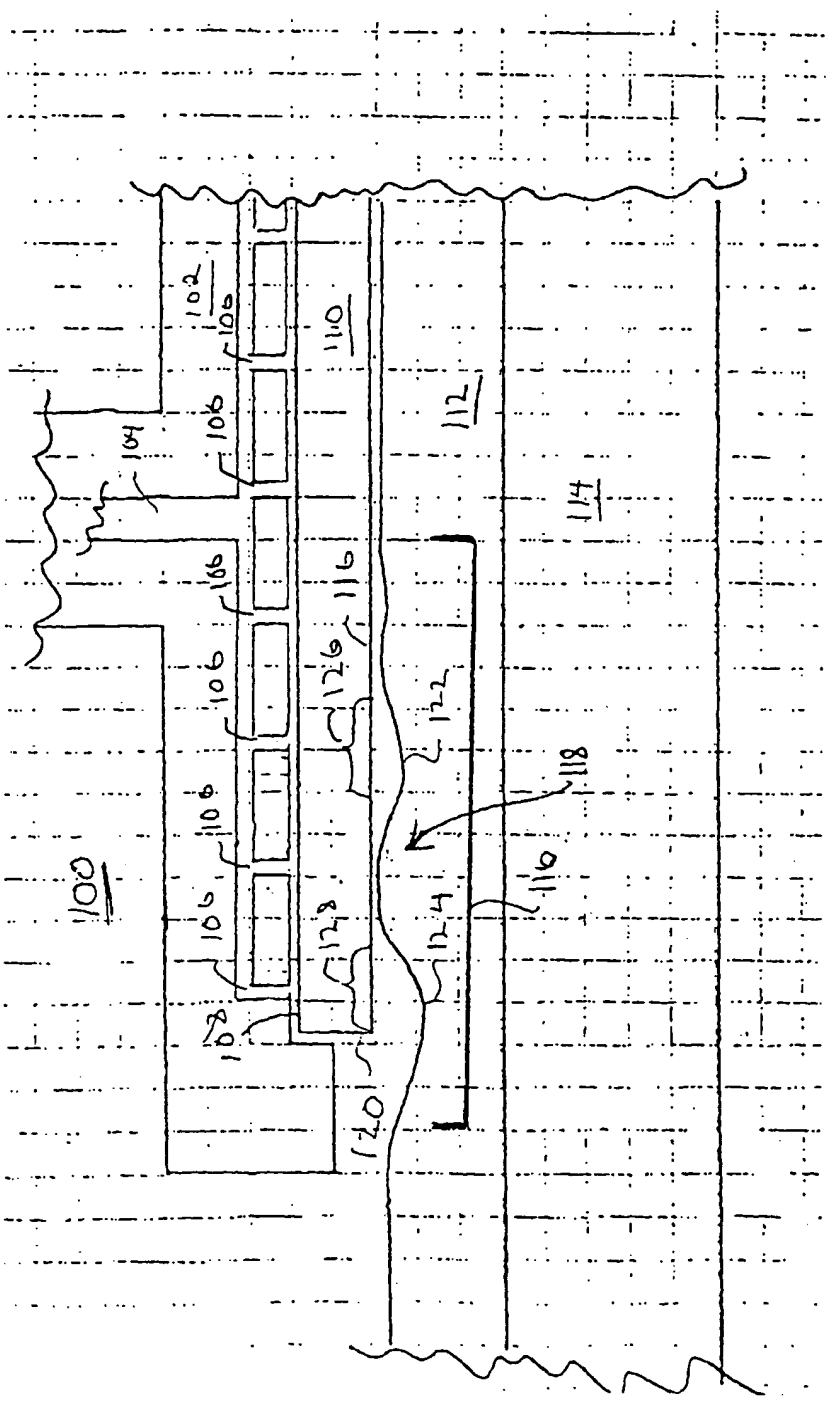
   a sensor arranged to detect changes in the shape of the polishing pad and wherein the sensor is connected to a control unit arranged to generate control signals for the deformation unit to deform the surface of the substrate (204).

8. Apparatus as claimed in Claims 5, 6 or 7, wherein the deformation means comprises a plurality of displacement elements (308, 310, 312, 314, 316).

9. Apparatus as claimed in Claim 8, wherein the plurality of displacement elements are arranged in a plurality of concentric rings.

10. Apparatus as claimed in Claims 5, 6, 7, 8 or 9, wherein the deformation means comprises at least one piezoelectric element.

Fig. 1



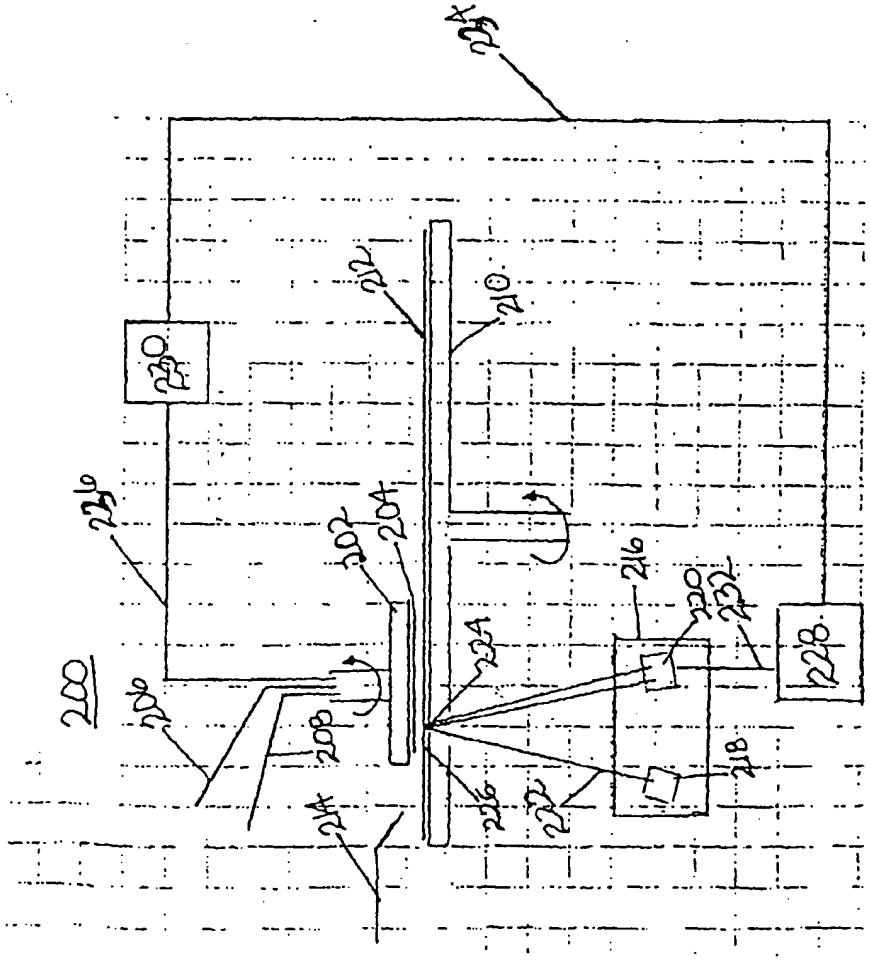

200
202
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FIG. 2

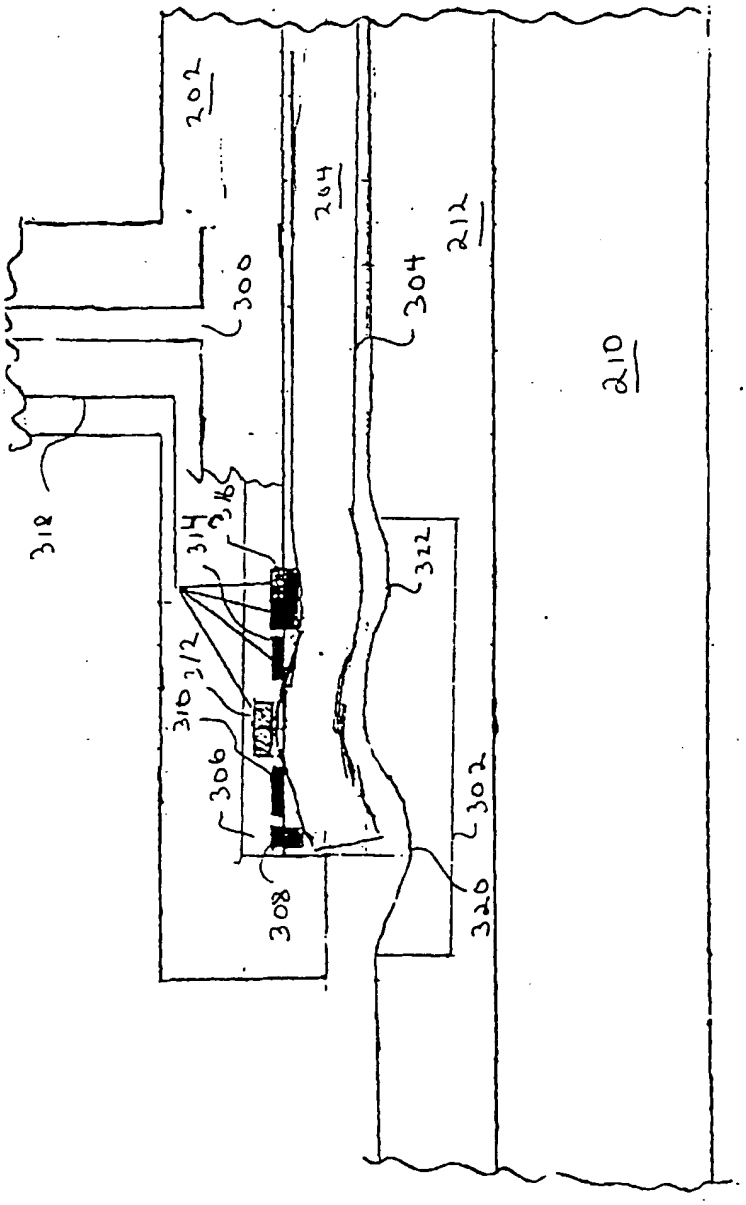


Fig. 3

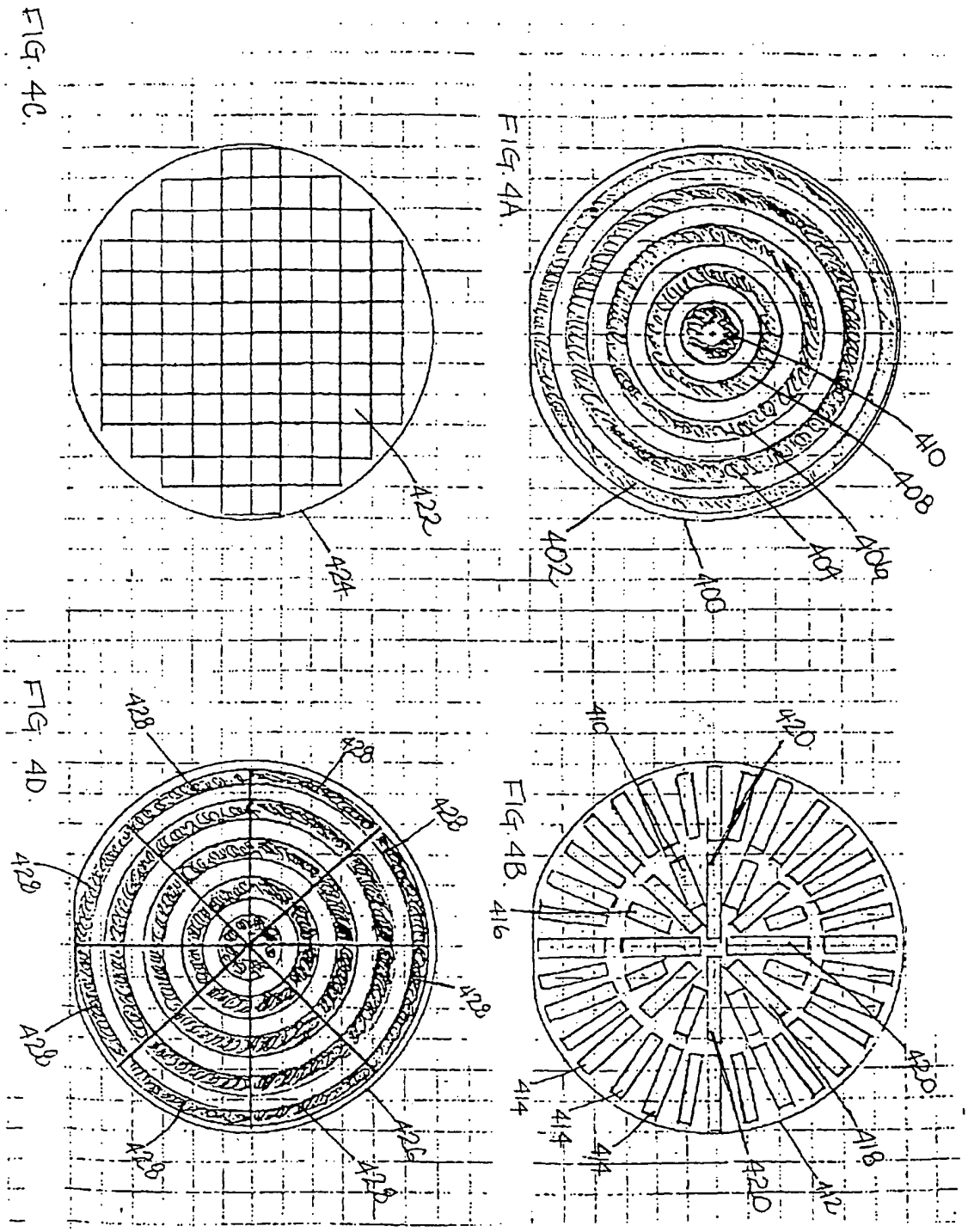
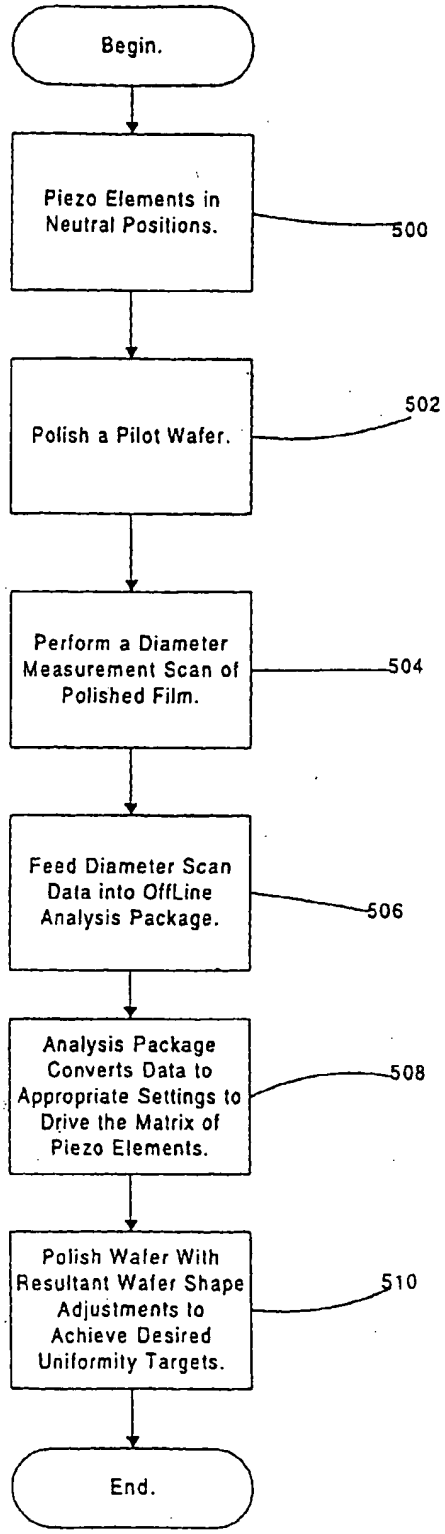


FIG. 4C.
422
424
FIG. 4A.
410
408
402
404
400
FIG. 4D.
428
426
FIG. 4B.
416
420
414
418
412

Fig. 5


Begin.
Piezo Elements in Neutral Positions.
500
Polish a Pilot Wafer.
502
Perform a Diameter Measurement Scan of Polished Film.
504
Feed Diameter Scan Data into OffLine Analysis Package.
506
Analysis Package Converts Data to Appropriate Settings to Drive the Matrix of Piezo Elements.
508
Polish Wafer With Resultant Wafer Shape Adjustments to Achieve Desired Uniformity Targets.
510
End.

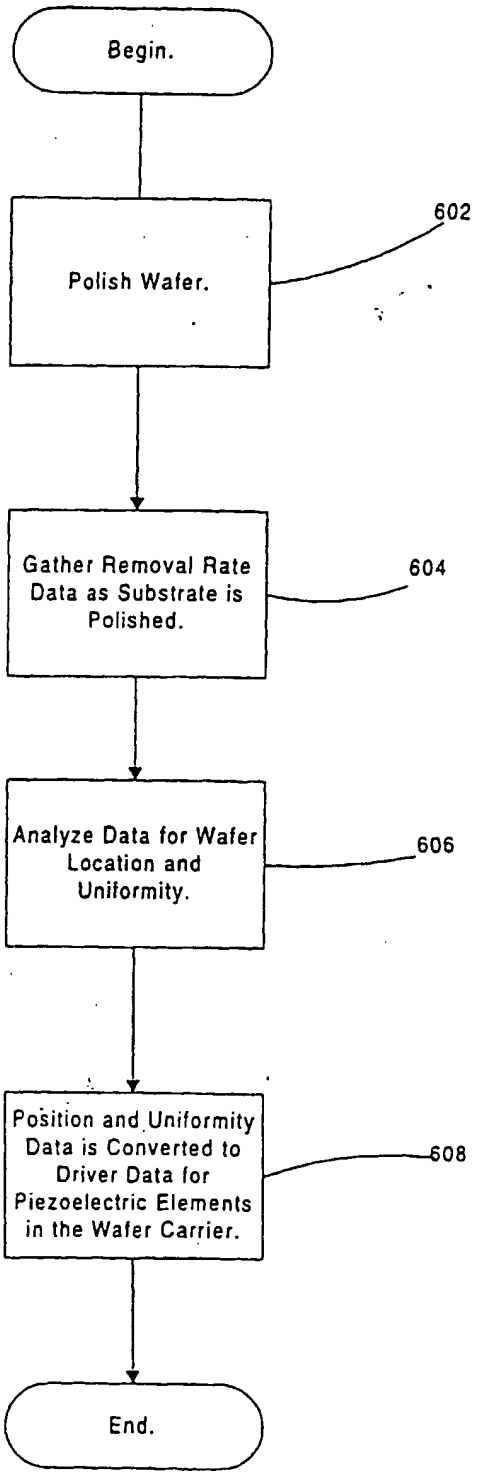

Begin.
Polish Wafer.
602
Gather Removal Rate Data as Substrate is Polished.
604
Analyze Data for Wafer Location and Uniformity.
606
Position and Uniformity Data is Converted to Driver Data for Piezoelectric Elements in the Wafer Carrier.
608
End.

Fig. 6

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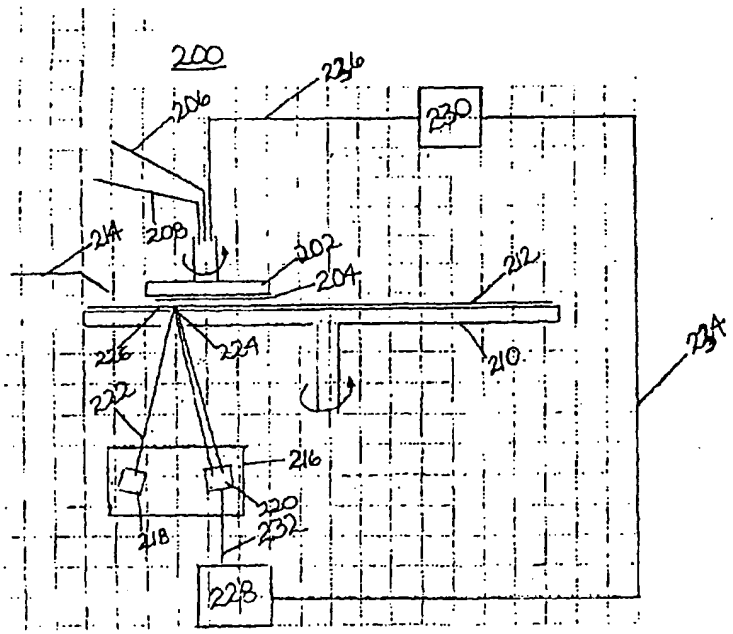

FIG. 2

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EUROPEAN SEARCH REPORT

Application Number
EP 98 30 7332

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 5 643 060 A (SANDHU ET AL.) 1 July 1997 (1997-07-01) * column 5, line 43 - column 7, line 30 * ---	1,5	B24B37/04 B24B41/06 B24B49/00 //H01L21/304
A	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 08, 29 September 1995 (1995-09-29) -& JP 07 130689 A (SONY CORP), 19 May 1995 (1995-05-19) * abstract; figures * ---	2,10	
A	US 5 635 083 A (BARNS ET AL.) 3 June 1997 (1997-06-03) * abstract; figures * -----	1,5	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

B24B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	25 September 2000	Garella, M

CATEGORY OF CITED DOCUMENTS

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